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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,217	11/01/2001	Craig Nemecek	CPPR-CD01207M	1780

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EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/002,217	NEMECEK, CRAIG	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 were rejected in office action of 17 November 2005.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 17 January 2006 has been entered.

Claims 1, 6, 14 have been amended. Claims 1-20 have been submitted for reconsideration. Claims 1-20 have been rejected.

Claim Rejections - 35 USC § 112

In response to the rejections of claims 1-20 under 35 U.S.C. § 112, first paragraph, in the previous office action, Applicants response invokes 35 U.S.C. § 112, sixth paragraph regarding claim 1. Applicants response has amended claims 6 and 14 to recite, inter alia, "detecting an I/O read instruction followed immediately by a conditional jump instruction." This embodiment conforms to the scope of invention described by the specification, in particular pages 26-29. The specification provides an example of an I/O read instruction followed immediately by a conditional jump instruction at page 26, lines 17-24.

Because 35 U.S.C. § 112, sixth paragraph, provides for a claim drafted in means or step for format "to be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof;" because Applicants' response specifically points to page 27, line 5 through page 28, line 8; and because claims 6 and 14 are supported by the same disclosure in accordance with 35 U.S.C. § 112, first paragraph; the limitation of claim 1 wherein "the virtual microcontroller having means for detecting an I/O read instruction followed by a conditional jump instruction" is interpreted as equivalent to the structure, material, or acts encompassed by the claim language of claims 6 and 14 reciting "detecting an I/O read instruction followed immediately by a conditional jump instruction."

If this interpretation of the limitations of claim 1, as prescribed by 35 U.S.C. § 112, sixth paragraph, is unduly narrow or inappropriate, Applicants' clarification is required. This clarification must include specific citation of support in the specification in compliance with 35 U.S.C. § 112, first and sixth paragraph, for which this interpretation is plainly inappropriate.

The previous rejections under 35 U.S.C. § 112, first paragraph, have been withdrawn in light of Applicants' amendments to the claims, invocation of 35 U.S.C. § 112, sixth paragraph, and the claim interpretation set forth above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1-4, 6-11, and 13-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,366,878 to Grunert in view of "Structured Computer Organization, Fourth Edition" by Andrew S. Tanenbaum with contributions by James R. Goodman (hereafter referred to as Tanenbaum).

Regarding claim 1, Grunert teaches:

An In-Circuit Emulation system [*"a circuit arrangement for in-circuit emulation"* (column 1, lines 66-67)], comprising:

A microcontroller [*"comprising a first ... microcontroller"* (column 1, line 66 – column 2, line 1)] having a microcontroller clock [*"a clock synchronizes the two microcontrollers (2, 3)"* (column 2, lines 58-59)]; and

A virtual microcontroller [*"comprising ... a second microcontroller"* (column 1, line 66 – column 2, line 1)] coupled to and executing instructions in lock-step with the microcontroller [*"a clock synchronizes the two microcontrollers (2, 3)"* (column 2, lines 58-59)] by executing the same instructions [*"The microcontrollers have an ROM memory 8, 8' in which the operating program is otherwise stored in normal operation. During in-circuit emulation, the memory 8, 8' is switch off... The master 2 is connected to the*

external memory 4 by means of its ports P0, P2... The data D read out from the memory 4 are also fed to the slave 3." (column 4, lines 29-53); That is, during in-circuit emulation, both microcontrollers (2, 3) receive the same operating program from external memory 4, thus execute the same instructions.] using the same clocking signals [*"A clock system 5 ensures good synchronization between master 2 and slave 3."* (column 5, lines 8-9); *"a clock synchronizes the two microcontrollers (2, 3)."* (column 2, lines 58-59)] and wherein the microcontroller sends I/O read data to the virtual microcontroller [*"The master 2 processes the operating program by evaluating the data, input externally via the ports P0, ..., P4, from the application system. Feeding the operating program to the slave 3 serves the purpose of properly timing the control of the data input and output via the ports P0', P2', P3'."* (column 4, line 67 – column 5, line5); I/O read data present in the operating program and evaluated by the master 2 is sent to the virtual microcontroller to also evaluate the same I/O read data].

Grunert does not expressly disclose the limitations regarding "means for detecting an I/O read instruction followed (immediately) by a conditional jump instruction, and for computing a conditional jump address prior to receipt of I/O read data from the microcontroller to remain in lockstep execution with said microcontroller, and further having means for determining after receipt of the I/O read data from the microcontroller whether to proceed with instruction execution at a next consecutive address or at the conditional jump address."

Tanenbaum teaches "Branch Prediction," (page 270, § 4.5.2). Tanenbaum teaches branch prediction for conditional branches [*"Consequently, what most machines do when they hit a conditional branch is predict whether it is going to be taken or not."* (page 272)]. Tanenbaum teaches "computing a conditional jump address prior (to execution of the jump instruction) [*"If a branch is correctly predicted, there is nothing special to do. Execution just continues at the target address."* (page 272); Here Tanenbaum clearly teaches that "execution just continues" because the target address of the branch instruction is already known, i.e. precomputed].

Tanenbaum expressly teaches motivation for implementing branch prediction [*"All computer manufacturers want their systems to run as fast as possible... Consequently, most of the ideas we will discuss are already in use in a wide variety of existing products."* (page 264); *"Early pipelined machines just* ***stalled*** *until it was known whether the branch would be taken or not. Stalling for three or four cycles on every conditional branch, especially if 20% of the instructions are conditional branches, wreaks havoc with performance."* (page 272); *"Clearly, having the predictions be accurate is of great value, since it allows the CPU to proceed at full speed."* (page 273)].

Tanenbaum and Grunert are both directed to processor architecture and are therefore analogous prior art.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention that I/O instructions are slow instructions that generally take "three or four cycles" or even longer. It would therefore be obvious to a person of ordinary skill in the art at the time of Applicants' invention, because of the teachings of Tanenbaum, that the

performance of a processor, in the case of Grunert a microcontroller, can be improved by using branch prediction where a branch instruction depends on the result of an I/O instruction. In addition to being "already in use in a wide variety of existing products," such an improvement would help the system to "run as fast as possible."

Therefore, upon identifying the synchronization problem where the virtual microcontroller executes an I/O read instruction immediately followed by a conditional branch (jump) instruction, it would have been obvious to a person of ordinary skill in the art to combine Tanenbaum's teaching of branch prediction to "compute a conditional jump address prior to receipt of I/O read data from the microcontroller to remain in lockstep execution with said microcontroller," thus helping the system to "run as fast as possible." As taught by Tanenbaum, branch prediction requires "means for determining whether to proceed with instruction execution at a next consecutive address or at the conditional jump address" (as cited above and exemplified on page 271).

Claim 2 recites an implicit limitation of claim 1. "Wherein the conditional jump address is computed while the I/O read data are sent from the microcontroller to the virtual microcontroller" is regarded as functionally equivalent to "computing a conditional jump address prior to receipt of I/O read data from the microcontroller" and "wherein the microcontroller sends I/O read data to the virtual microcontroller."

Regarding claims 3 and 4, Tanenbaum teaches an instruction wherein the processor sets a zero flag if an I/O read test condition is met [*"The next two groups deal with testing and*

comparing, and then jumping based on the results. The results of test and compare instructions are stored in various bits of the EFLAGS register. Jxx stands for a set of instructions that conditionally jump, depending on the results of the previous comparison (i.e., the bits in EFLAGS)." (page 360)]. The limitation "wherein the jump conditions is met if the zero flag is set" is taught by Tanenbaum (page 360) especially when read by one of ordinary skill in the art. This claim describes a "jump if zero" or JZ assembly instruction.

Claim 6 recites a method performed by the system of claim 1. Claim 6 is therefore rejected for rationale similar to that given above regarding claim 1.

Claims 7 and 8 recite limitations implicit in claim 6. Claims 7 and 8 recite "executing a next consecutive instruction" and "executing an instruction at the conditional jump address" based on whether the conditional jump condition is met, as appropriate. These limitations are implicit from claim 6, reciting "a method of handling conditional jumps in the virtual microcontroller." Failure to perform the steps of claims 7 and 8 would render the system of claim 6 inoperative. Therefore, claims 7 and 8 are rejected for rationale similar to that given above regarding claim 6.

Claim 9 recites limitations that correspond to claim 2. Claim 9 is therefore rejected for rationale similar to that given above regarding claim 2.

Claims 10 and 11 recite limitations that correspond to claims 3 and 4. Claims 10 and 11 are therefore rejected for rationale similar to that given above regarding claims 3 and 4.

Regarding claim 13, Tanenbaum teaches that the method is stored as instructions for execution by a programmed processor [*"A different way to go is to have the compiler help out."* (page 275)].

Claim 14 recites a method corresponding to claim 6 wherein "microcontroller" is replaced by "device under test." As a microcontroller in the claimed system constitutes a "device under test," claim 14 is rejected for rationale similar to that given above regarding claim 6.

Claims 15-19 recite limitations that correspond to claims 7-11. Claims 15-19 are therefore rejected for rationale similar to that given above regarding claims 7-11.

2. Claims 5, 12, and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Grunert in view of Tanenbaum as applied to claims 1 and 6 above, and further in view of US Patent No. 6,173,419 to Barnett.

Neither Grunert nor Tanenbaum expressly teach that the virtual microcontroller is implemented in a field programmable gate array (FPGA).

Barnett teaches the use of an FPGA as a hardware emulator (abstract; column 2, lines 11-16; column 5, lines 38-56). Barnett teaches that the advantage of such an arrangement is the reuse of the hardware emulator for different configurations (column 2, lines 41-51).

Barnett, Tanenbaum, and Grunert are all directed to processor architecture and are therefore analogous prior art.

Therefore, it would have been obvious for a person of ordinary skill in the art at the time of Applicants' invention to implement the slave microcontroller taught by Grunert in an FPGA, according to the method taught by Barnett, in order to provide an in-circuit emulator system that facilitates emulating the emulated microcontroller in different configurations of target circuitry. Barnett expressly provides motivation for doing so [*"What is needed is an emulator for debugging software that operates in real time, is economical to create, and may be programmed to have a variety of configurations."* (column 2, lines 6-9)]. The combination could be achieved by implementing the slave microcontroller taught by Grunert as emulated by an FPGA connected to and configured by the host computer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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3/29/06